

FIG. 1C

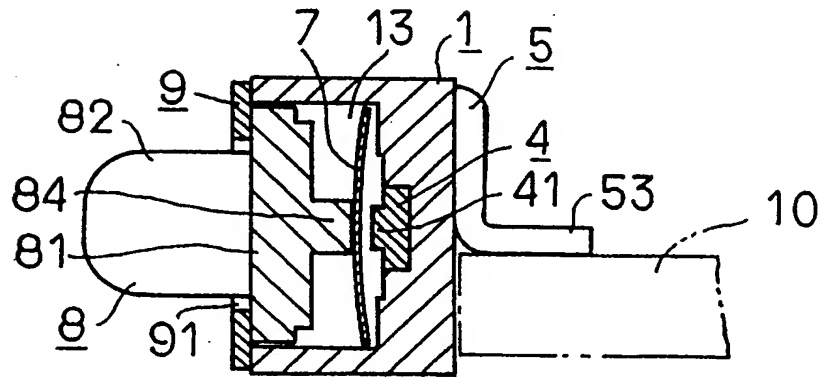


FIG. 2

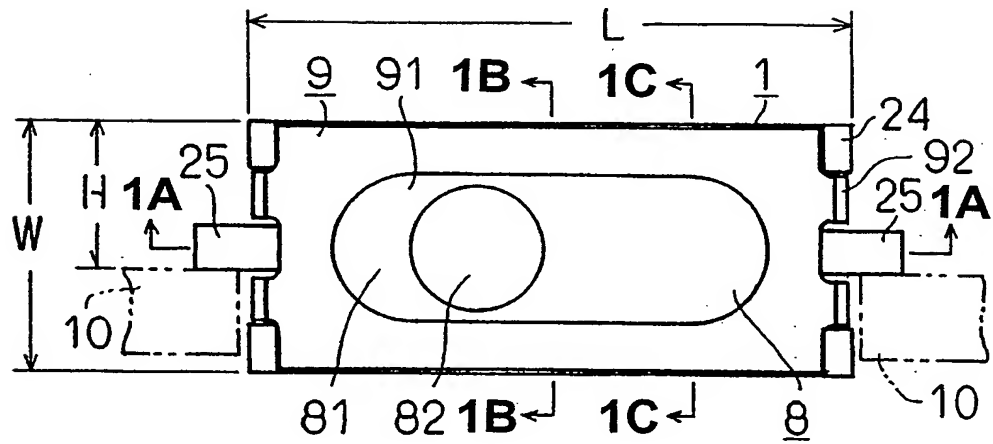


FIG. 3

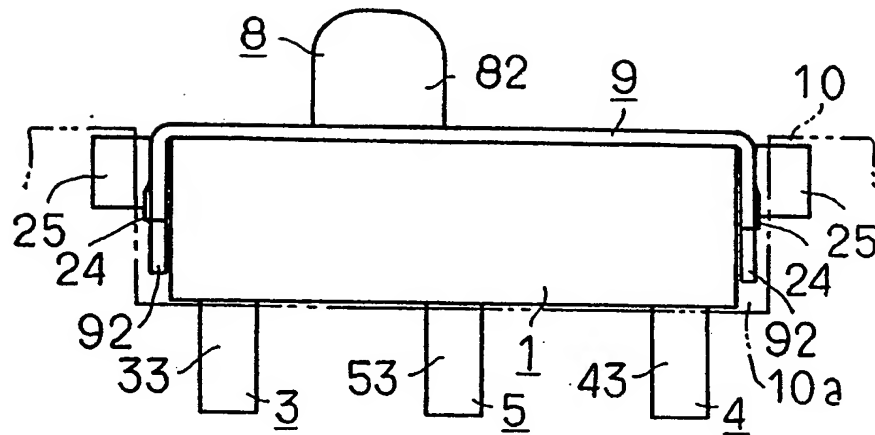


FIG. 4

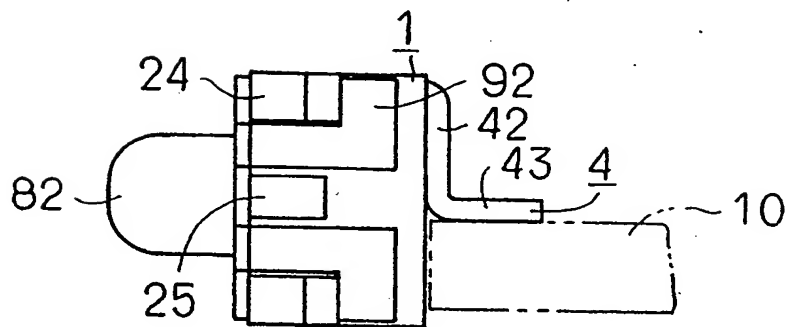


FIG. 5

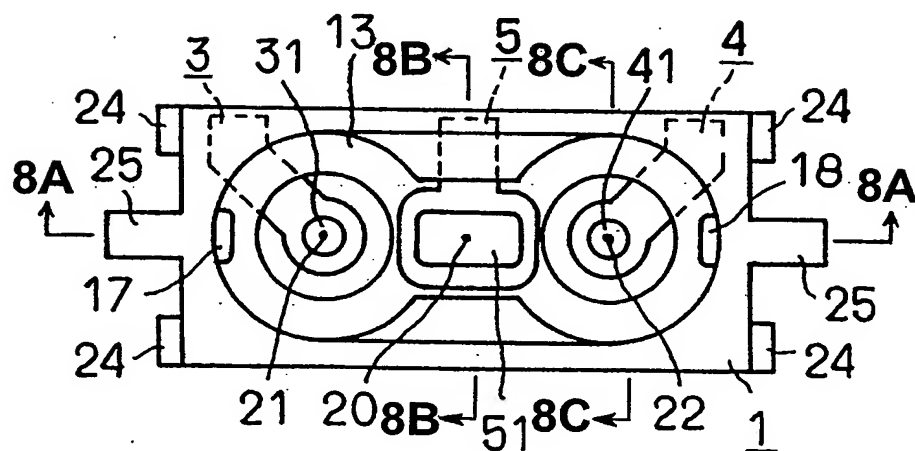
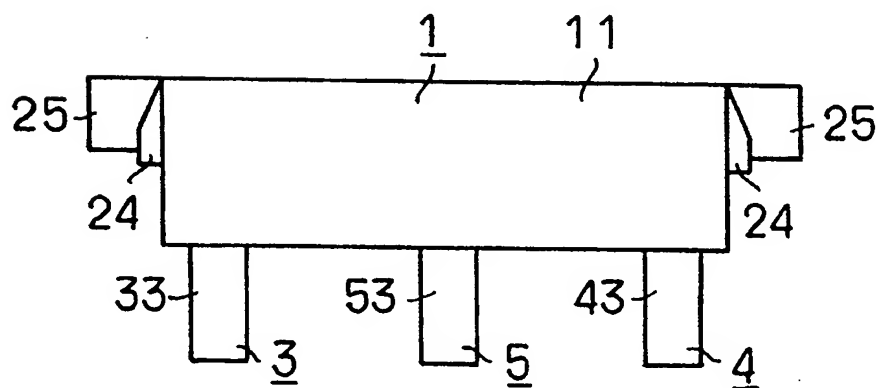


FIG. 6



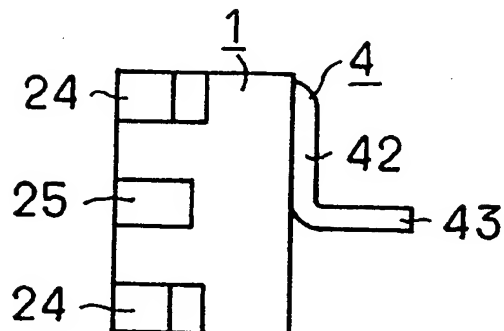


FIG. 7

FIG. 8A

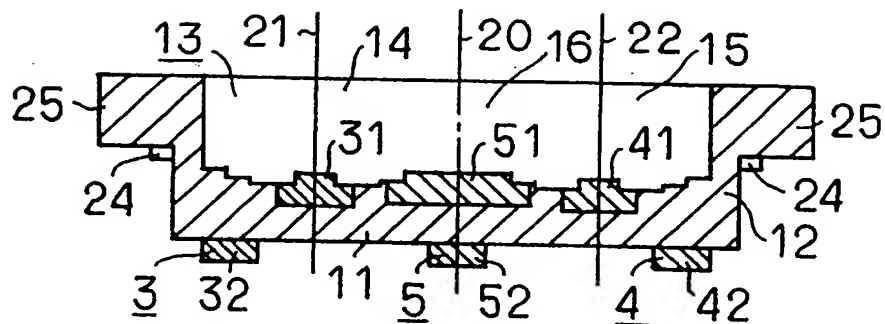
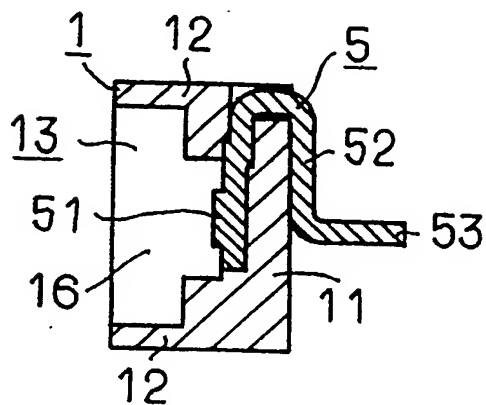


FIG. 8B



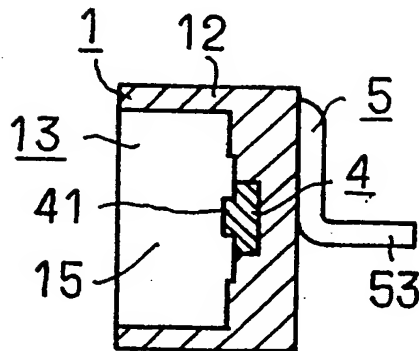


FIG. 8C

FIG. 9A

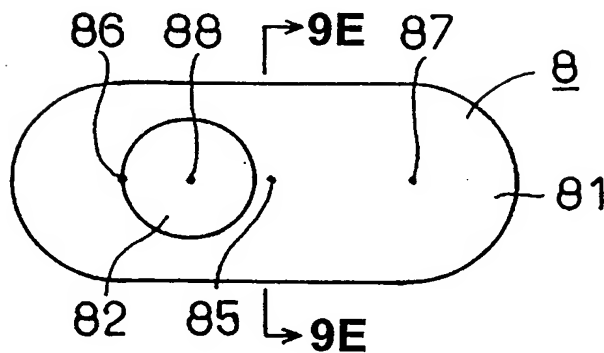


FIG. 9B

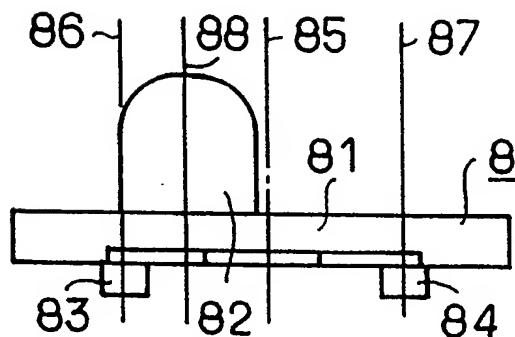


FIG. 9C

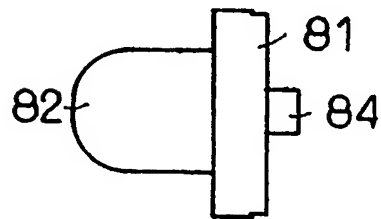
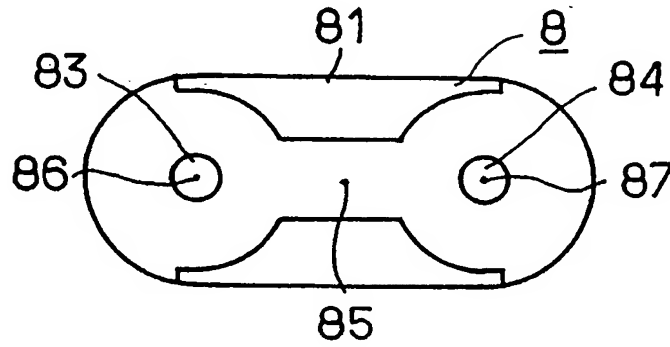


FIG. 9D

FIG. 9E

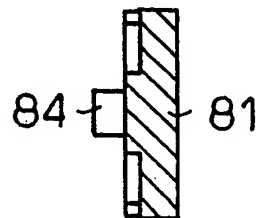


FIG. 10A

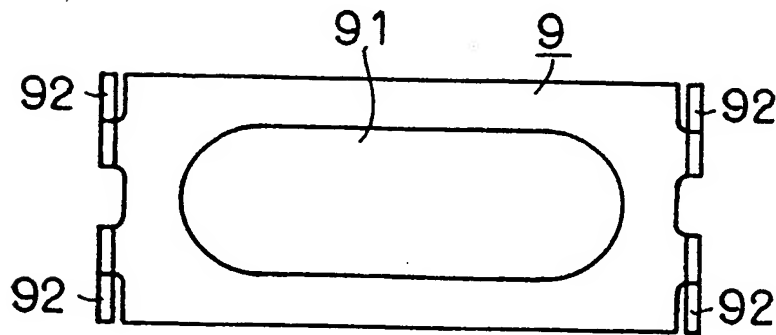


FIG. 10B

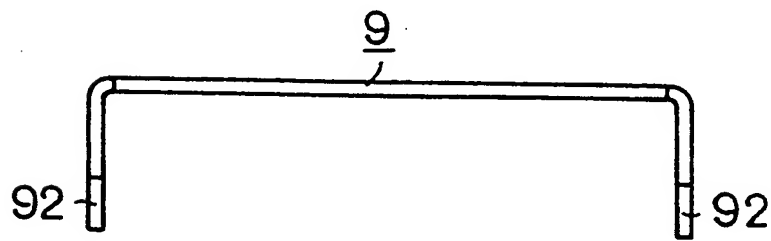


FIG. 10C

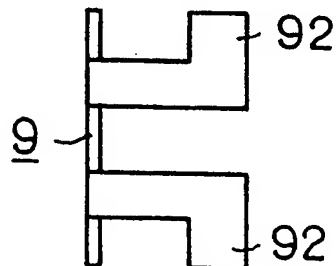


FIG. 11A

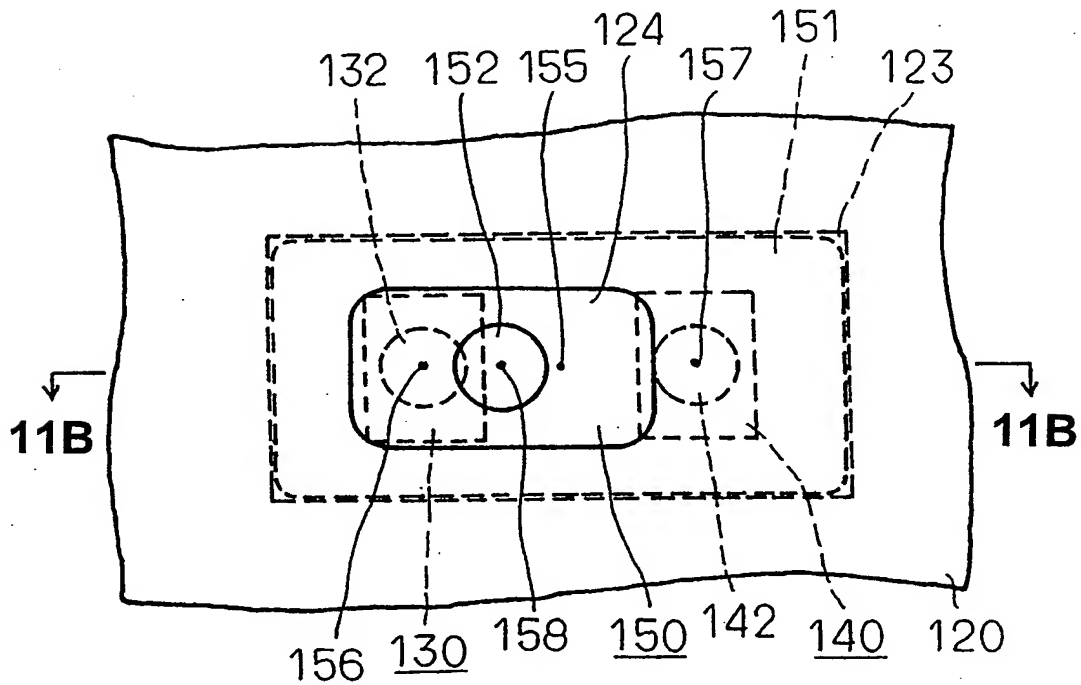
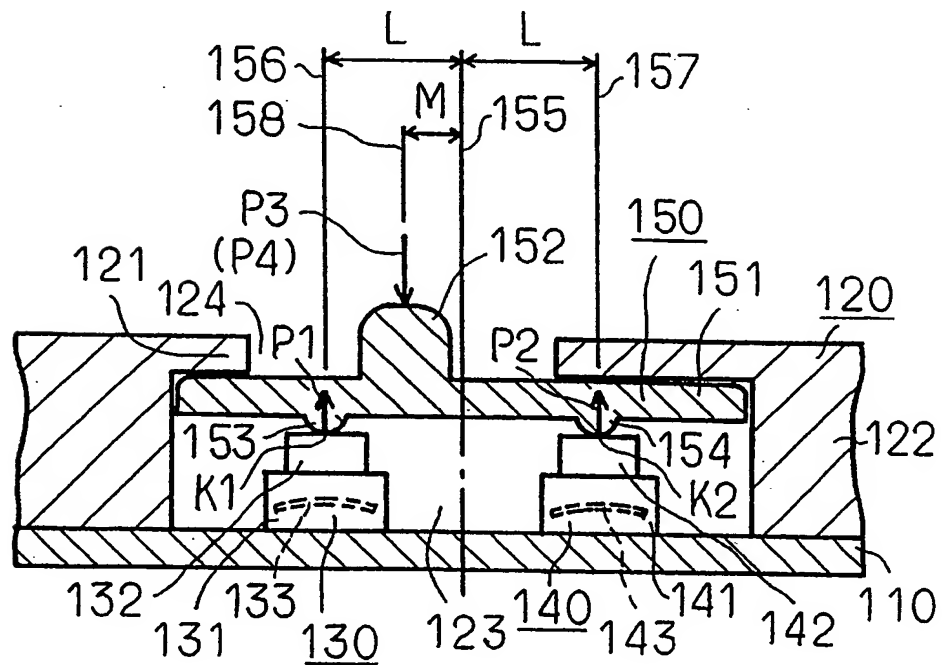


FIG. 11B



This diagram shows a cross-sectional view of a semiconductor device. A substrate 150 is shown with a central region 151. Two semiconductor elements, K1 and K2, are mounted on the substrate. K1 is on the left and K2 is on the right. They are connected to a common bus 152. The bus is connected to a power supply 153. The substrate has a central region 151 and two side regions 155 and 157. The distance between the elements is labeled M. The distance from the center to the side regions is labeled L. The substrate has a central region 151 and two side regions 155 and 157. The distance between the elements is labeled M. The distance from the center to the side regions is labeled L.

FIG. 13
PRIOR ART

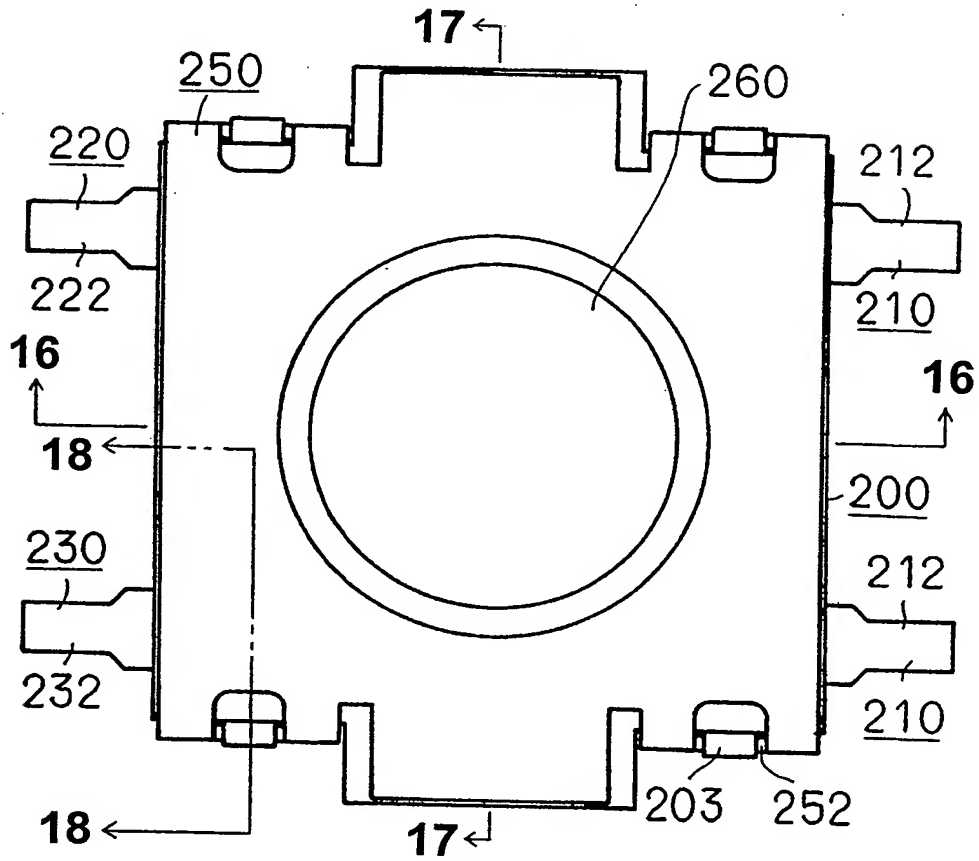
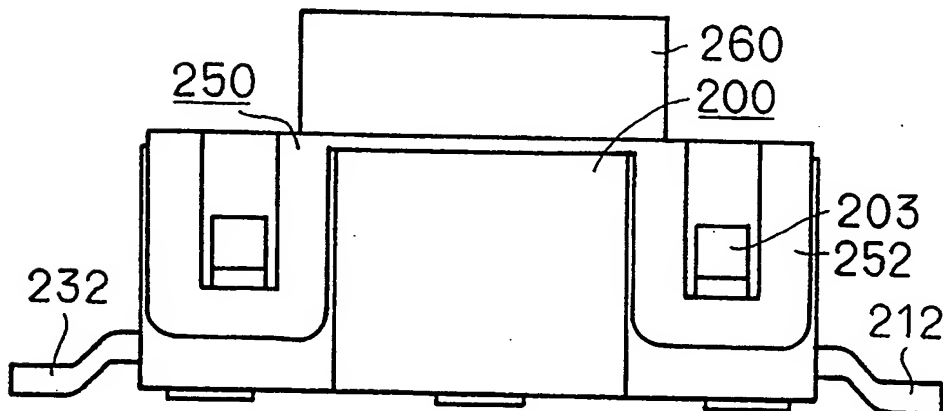


FIG. 14
PRIOR ART



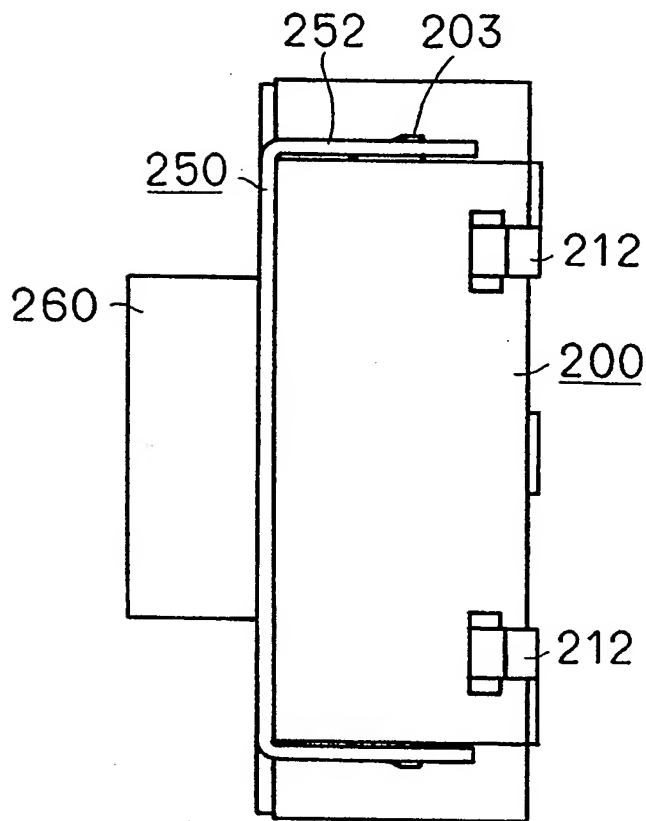


FIG. 16
PRIOR ART

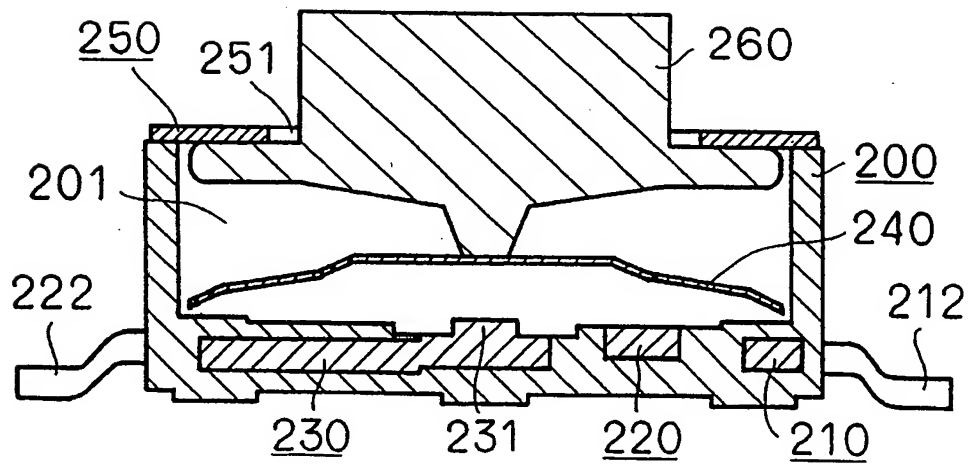


FIG. 17
PRIOR ART

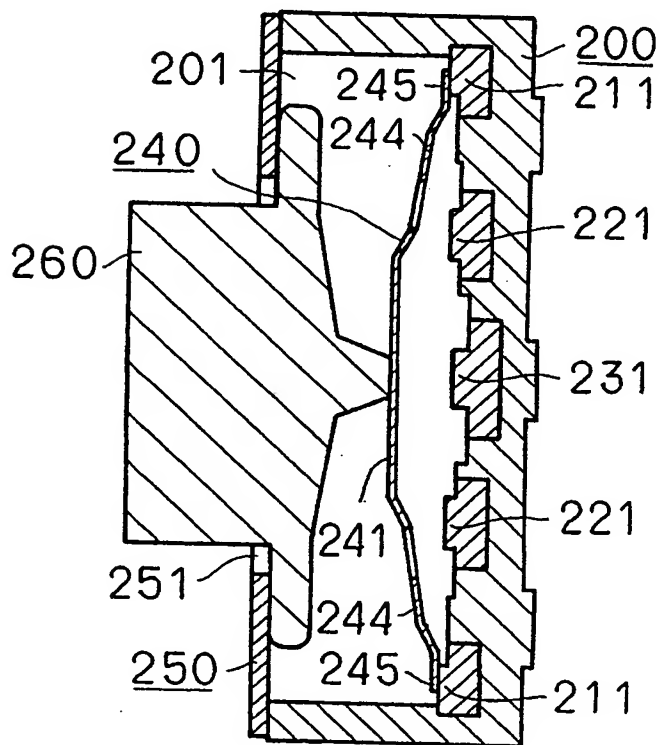


FIG. 18
PRIOR ART

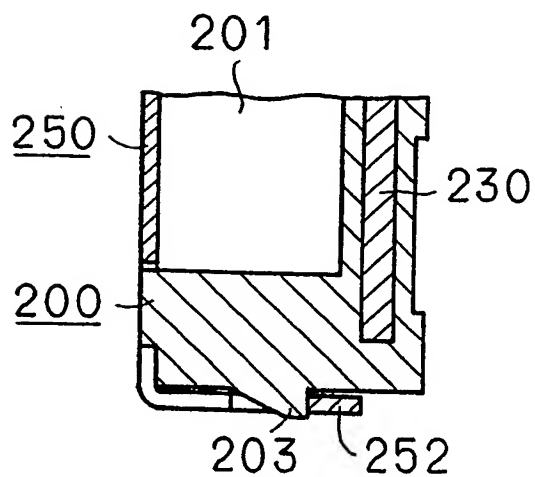


FIG. 19A
PRIOR ART

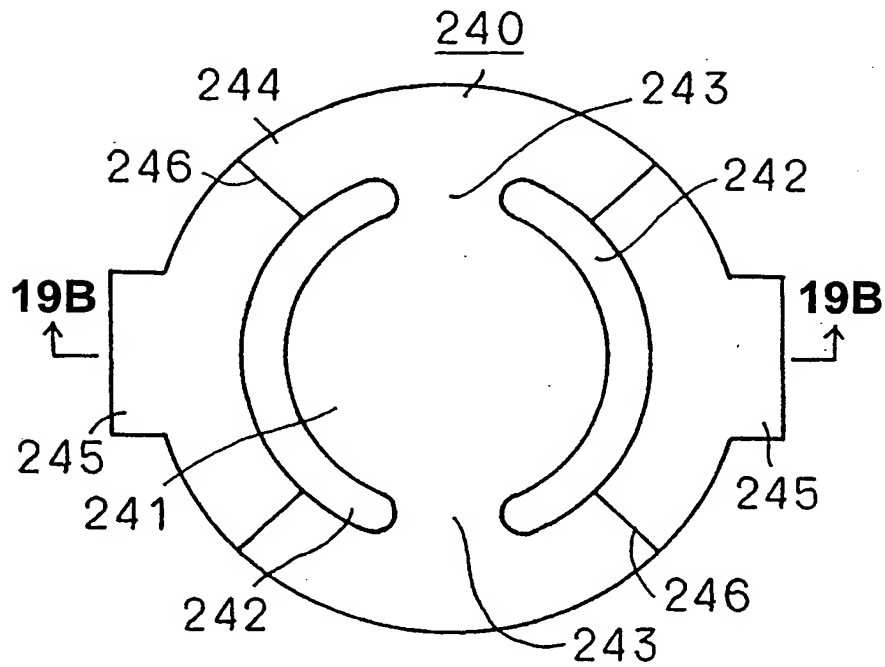


FIG. 19B
PRIOR ART

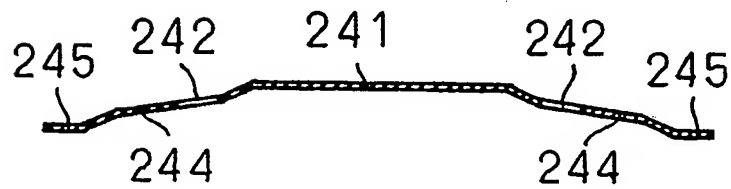


FIG. 20
PRIOR ART

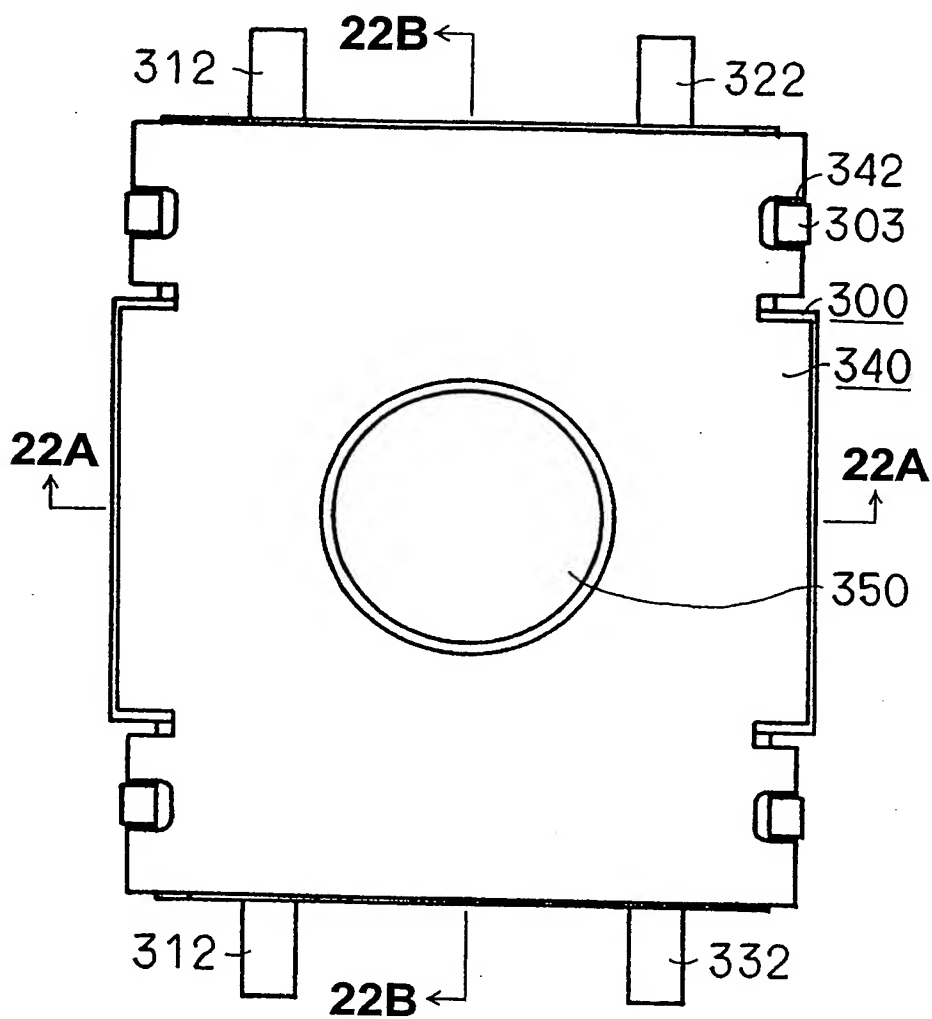


FIG. 21
PRIOR ART

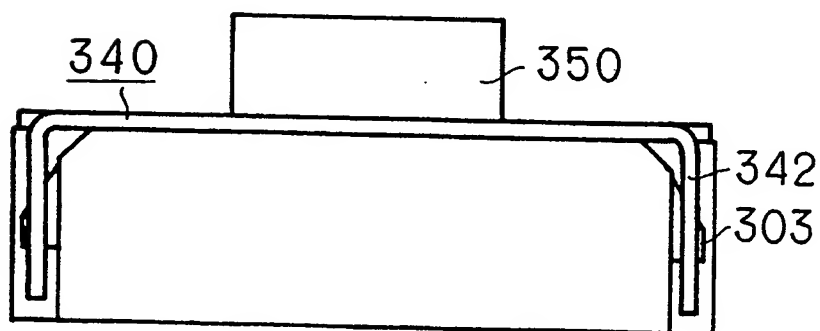


FIG. 22A
PRIOR ART

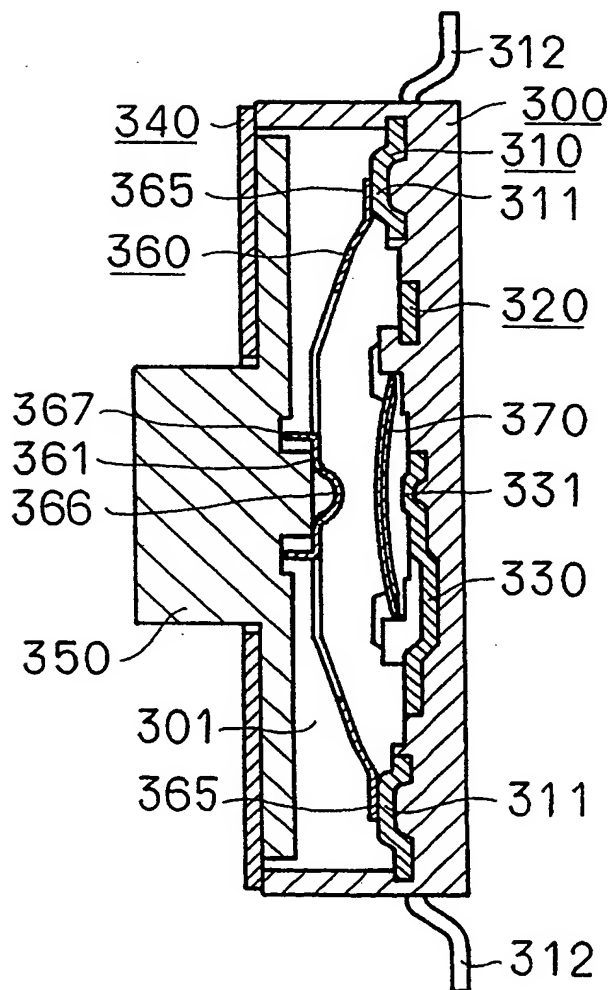
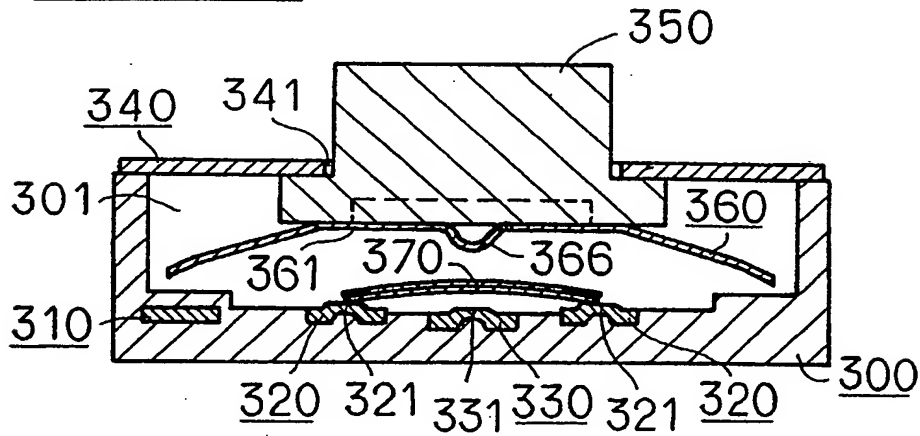


FIG. 22B
PRIOR ART

FIG. 23
PRIOR ART

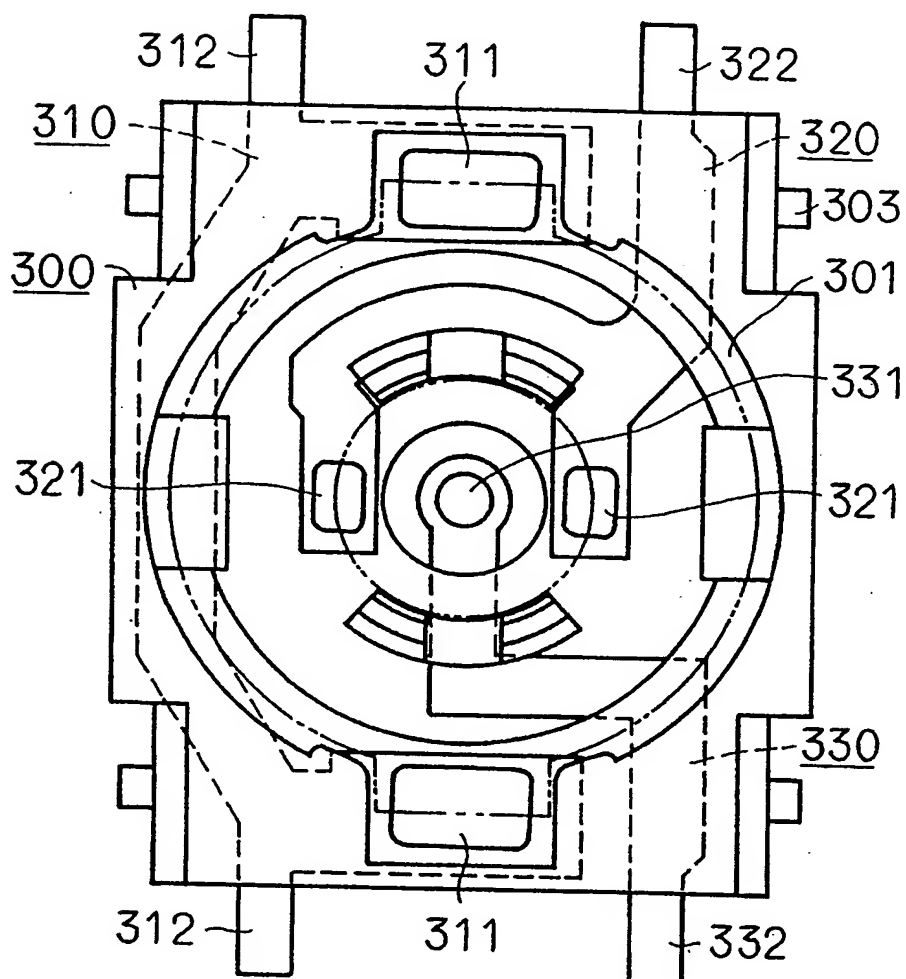


FIG. 24
PRIOR ART

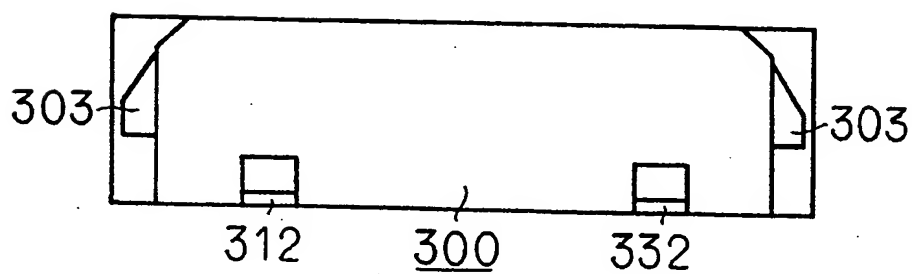


FIG. 25
PRIOR ART

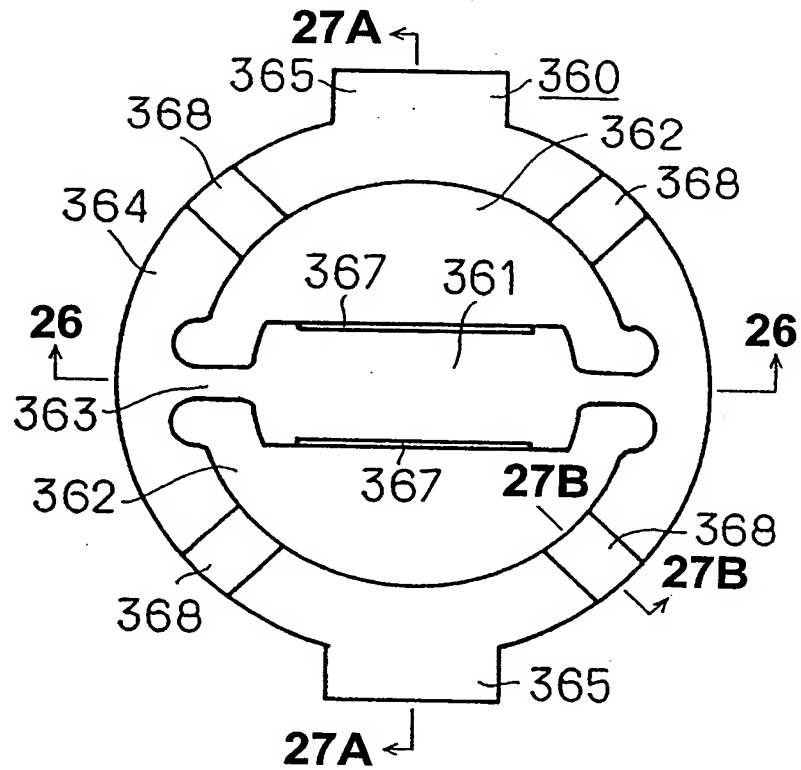
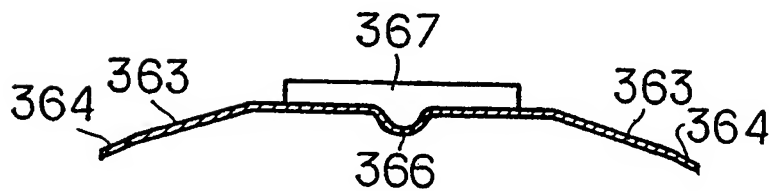


FIG. 26
PRIOR ART



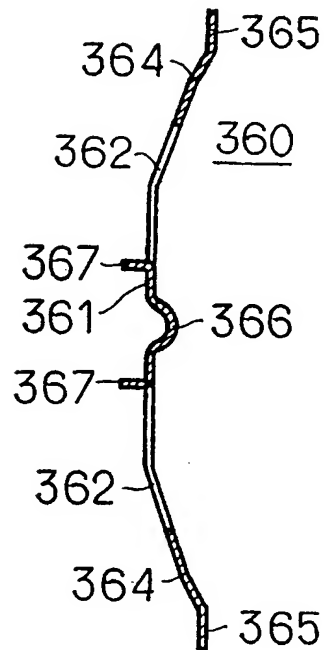


FIG. 27A
PRIOR ART

FIG. 27B
PRIOR ART

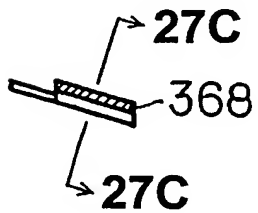


FIG. 27C
PRIOR ART

